Implementing Twisted Pair Transceivers with NEURON® CHIPS

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Introduction

LONWORKS technology supports several communications media including twisted pair cable, radio, and power line. Twisted pair wiring offers several advantages for typical control applications. The cable is readily available in shielded and unshielded versions, for plenum and non-plenum applications. Relative to fiber optic and coaxial cable, twisted pair cable is inexpensive, simple to work with, and easily maintained.

Echelon offers a wide range of twisted pair control modules that incorporate a NEURON® CHIP, PROM socket, twisted pair communication transceiver, and connectors for power, I/O, and the two wire network data bus. The small size of these modules permits them to be mounted on or inside a customer's product, directly adjacent to the sensors, outputs, or displays that the module will control.

Using an Echelon twisted pair control module can save literally hundreds of hours of development time compared with a custom-designed module. The modules are designed to be both FCC and VDE compliant, eliminating time consuming and expensive laboratory testing, component selection, and layout redesign work by the customer. As UL Recognized components, the modules can be integrated into a product without further safety testing. The modules are interchangeable with other Echelon twisted pair control modules, and allow the user to change communication speeds and transceivers without developing new modules. Finally, the modules are economically priced for both low and high volume users.

There may be situations in which an Echelon twisted pair control module is not the best solution due to size restrictions or government local content legislation. This document is intended for those who cannot use an Echelon twisted pair control module, and who wish to implement their own twisted pair transceiver. Four transceiver designs are described below. These include:

- Differential direct-connect
- EIA RS-485
- Transformer isolated 78 kilobits per second (kbps)
- Transformer isolated 1.25 megabits per second (Mbps)

Each transceiver has specific limitations associated with its design. These limitations include the total number of nodes that can be interconnected, distance between nodes, total network wire length, characteristics of the wire, response time of busy networks, electrical isolation, and transceiver cost. The reader should carefully review the specifications of the transceivers listed in the following pages and select the transceiver design that best meets the application requirements.

This document includes schematics for the transceivers, as well as component specifications and sources for hard-to-find items. The user should note that it will probably be necessary to change, add, or delete some components, or to change the topology in which they are mounted, in order to comply with FCC requirements. The designer should therefore plan to undertake a technical review of the suitability of the attached schematics for each specific application, and to make part and topology changes as required.

The LONBUILDER™ Twisted Pair Transceiver allows users to develop and debug LONWORKS networks using twisted pair media. This product is available from Echelon in the LONBUILDER Developer's Workbench family of development products and serves as a convenient evaluation tool for twisted pair transceiver development and testing.

Additional References

The reader will find additional pertinent information in the following Echelon documents:

- *Optimizing LONTALK£™ Response Time* Engineering Bulletin (Part No. 005-0011-01)
- *NEURON® CHIP Advance Information* (Part No. 005-0018-01 Rev. B)
- *Enhanced Media Access Control with Echelon's LONTALK™ Protocol* Engineering Bulletin (Part No. 005-0001-01)

NEURON CHIP Communication Port Interface

Introduction

The five-pin network communications port on the NEURON CHIP allows it to be interfaced to a wide variety of network transceivers. The communications port may be configured to operate in differential, single-ended, or special purpose mode. The differential and single-ended modes are used for twisted-pair transceivers. The special-purpose mode is designed for use with special transceivers that use more complex modulation and demodulation schemes. The following sections focus on the differential and single-ended modes.

A Typical LONWORKS Message

The NEURON CHIP communications port encodes transmitted data and decodes received data using biphase space coding, also known as differential Manchester coding. This coding scheme guarantees a transition in every bit period for the purpose of synchronizing the receiver clock. Zero/one data are indicated by the presence or absence of a second transition halfway between clock transitions. A mid-cell transition indicates a zero, while the lack of a mid-cell transition indicates a one. Differential Manchester coding is polarity-insensitive, and change of polarity in the Manchester encoded data will not affect its interpretation. Figure 1 illustrates a typical packet transmitted by the NEURON CHIP.

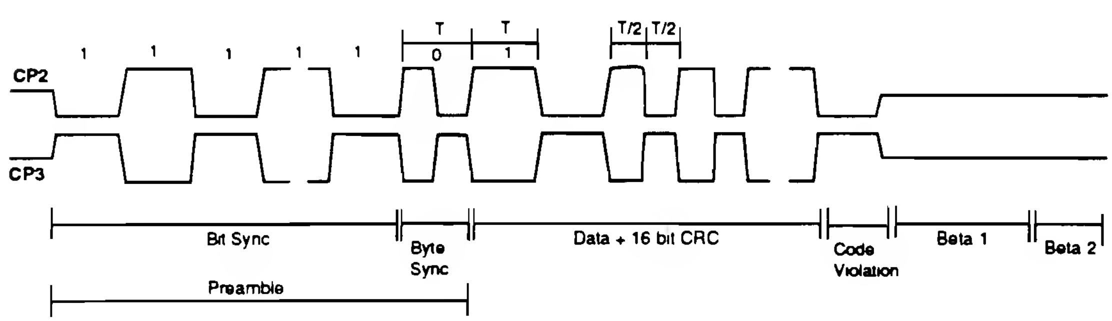


Figure 1. Waveform of a Typical NEURON CHIP Packet

The transmitter broadcasts a *preamble* at the beginning of a packet to allow the other nodes to synchronize their receiver clocks. The preamble consists of a series of Manchester ones, and its duration is at least eight bits long and is programmable by the user. The preamble is followed by a single byte-sync bit, which marks the start of byte boundaries at the bit following it. The byte-sync bit is a Manchester zero.

The NEURON® CHIP terminates the packet by holding the lines at the levels resulting from the last data bit for 2 to 2-1/2 bit times, and then tristates the line. The process of holding the data lines at fixed levels for 2 to 2-1/2 bit times causes a Manchester code violation, which signifies an end-of-packet condition to the receiving NEURON CHIP. *Beta 1* time is the idle period after a packet has been sent. The number of priority slots is defined by the *Beta 2* time. This number varies dynamically from 16 to 1024, depending on network traffic.

NEURON CHIP Communications Port Electrical Specifications

Table 1 summarizes the specifications for the NEURON CHIP communication port differential receiver.

Table 1. NEURON CHIP Communication Port Differential Receiver Electrical Specifications

	Min	Typical	Max
Common-Mode range, with specified hysteresis	1.2V		V_{dd}-2.2V
Common-Mode range with unspecified hysteresis	0.9V		V_{dd}-1.75 V
Input offset voltage	-0.05*V_h-35mV		0.05*V_h+35mV
Propagation delay ($V_{id}=V_{hyst}/2$ + 200mV)			230 ns
Input resistance	5 MΩ		
Wake up time			10 µs
Receiver supply current ($V_h=V_{dd}$) Receiver supply current ($V_h=0.125V_{dd}$)		245µA 145µA	575µA 375µA
Filter asymmetry (t_{plh}/t_{phl})	0.7		1.42

Figure 2 shows a block diagram of the receiver circuitry within the NEURON CHIP.

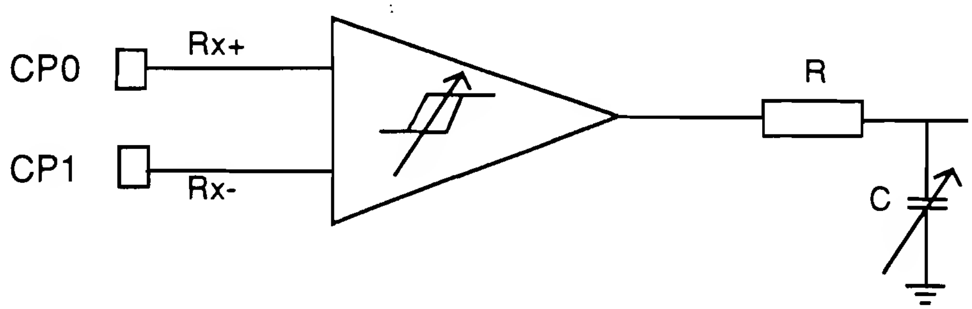


Figure 2. NEURON® CHIP Differential Input Receiver Circuit

The receiver circuitry consists of a comparator with programmable hysteresis. The inputs to the receiver are connected to CP0-CP1 of the communications port. The adjustable hysteresis allows the node to be tailored to the noise level present. The comparator is followed by a post-hysteresis programmable low-pass filter for suppressing transients. Eight different values of hysteresis can be selected for the CP0 and CP1 inputs. In the LONBUILDER Developer's Workbench, the screen supporting selection of the transceiver-specific parameters allows selection of the hysteresis value. These options are listed in Table 2. As a guideline, the minimum detectable signal is typically two to four times the value of the hysteresis value. Low values of hysteresis increase the minimum signal amplitude that can be detected and hence increase the transmission distance, but at the cost of increasing susceptibility to line noise.

One method of threshold selection would be to establish a worst-case noise environment and then adjust the threshold to a value which just avoids triggering the receiver on noise. A second method would be to set the threshold to about one quarter of the signal's peak-to-peak amplitude at the receiver, allowing some margin for inter-symbol interference and avoiding excessive timing jitter caused by detection at extremes on the receive waveform.

Table 2. Hysteresis Value Options As Fractions of the Differential Peak-to-Peak Voltage

Hysteresis	Min (V)	Typ (V)	Max (V)
0	0.019Vdd	0.027Vdd	0.035Vdd
1	0.040Vdd	0.054Vdd	0.068Vdd
2	0.061Vdd	0.081Vdd	0.101Vdd
3	0.081Vdd	0.108Vdd	0.135Vdd
4	0.101Vdd	0.135Vdd	0.169Vdd
5	0.121Vdd	0.162Vdd	0.203Vdd
6	0.142Vdd	0.189Vdd	0.236Vdd
7	0.162Vdd	0.216Vdd	0.270Vdd

Table 3 shows the values of the post-hysteresis filter that can be selected by the LONBUILDER Developer's Workbench during custom transceiver development. The purpose of the filter is to eliminate any short noise pulses from the incoming signal so that ones are not interpreted as zeros and zeroes as ones. The filter effectively eliminates very short pulses that are not part of the normal data transitions.

The LONBUILDER twisted pair transceiver uses filter value options zero for 1.25Mbps operation, and one for 78kbps operation.

Table 3. Receiver Filter Values

Option	Min (ns)	Typ (ns)	Max (ns)
0	2	6	9
1	90	270	580
2	200	535	960
3	410	1070	1920

In order for the receiver to detect the edge transitions, two windows are set up for each bit period T. The first window is set at T/2 and determines if a zero is being received. The second window is set at T and defines reception of a one. This transition then establishes the next two windows (T/2' and T'). If no transition occurs, a Manchester code violation is detected and the packet is assumed to have ended. Table 4 shows the width of this window as a function of the ratio of the NEURON CHIP input clock (in MHz) and the network bit rate (Mbps). A transition

will not be detected if it falls outside of either window. Any instability in the NEURON CHIP 's clock or oscillator directly affects the stability and position of the window. The jitter tolerance windows are expressed as fractions of the bit period T.

Table 4. Receiver Jitter Tolerance Windows

Ratio of NEURON CHIP Input Clock and Network Data Rate	Next Data Edge			Next Clock Edge		
	Min	Nom	Max	Min	Nom	Max
8:1	0.375T	0.500T	0.622T	0.875T	1.000T	1.122T
16:1	0.313T	0.500T	0.585T	0.813T	1.000T	1.185T
32:1	0.345T	0.500T	0.672T	0.845T	1.000T	1.155T
64:1	0.330T	0.500T	0.702T	0.830T	1.000T	1.170T
128:1	0.323T	0.500T	0.695T	0.382T	1.000T	1.177T
256:1	0.313T	0.500T	0.690T	0.818T	1.000T	1.182T
512:1	0.315T	0.500T	0.687T	0.815T	1.000T	1.185T
1024:1	0.315T	0.500T	0.687T	0.815T	1.000T	1.185T

NEURON CHIP Transmit Circuitry

Figure 3 shows the transmitter circuitry internal to the NEURON CHIP. NEURON CHIP pins CP2 and CP3 provide the differential driver output. CP2 and CP3 are in a high impedance state when the NEURON CHIP is in receive mode, and output complementary differential Manchester encoded signals while transmitting. With 40mA sink and source capability, the rise time of the outputs on CP2 and CP3 may require wave-shaping circuitry in order to control RFI emissions on the twisted pair data communication line.

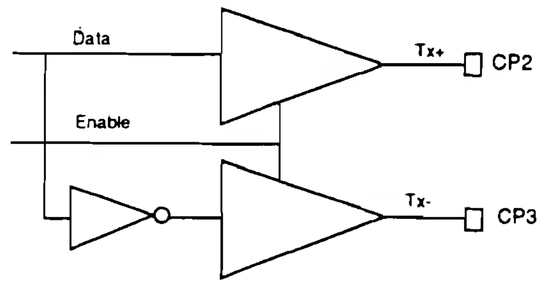


Figure 3. NEURON CHIP Transmit Circuit

Twisted Pair Medium Characteristics

Introduction

When transmitting digital information on twisted pair wire, consideration must be given to analog circuit and transmission line issues. Even when distances are short and bit rates are low, factors such as driver output impedance, receiver input impedance, receiver sensitivity, and cable impedance affect waveform integrity and ultimately data integrity. As the bit rates increase and/or the communication distance is increased, transmission line analysis techniques must be employed to analyze the distributed effects of resistance, inductance and capacitance along the cable.

Twisted Pair Cable as a Transmission Line

A useful rule of thumb is that accurate analysis of signal fidelity requires transmission line analysis when the round-trip propagation delay of the cable is longer than the rise time of the driving source. Table 5 lists the distance for which a twisted pair cable behaves like a transmission line for various bit rates, assuming that the rise time of the driving source is limited to 1/5th of a bit time. Due to the relative dielectric constant of the insulation material, the propagation speed through the cable will be less than the speed of light in a vacuum *c*. Typical twisted pair cable propagation speeds are about 0.65c. A speed of 0.667c is assumed in calculating the tabulated values.

Table 5. Twisted Pair Cable Transmission Line Behavior

Bit Rate (kbps)	Assumed Risetime (μs)	Minimum Distance (m)	Minimum Distance (ft)
4.88	40.9	4,096	13,000
9.8	20.5	2,048	6,700
19.5	10.3	1,028	3,300
39	5.12	512	1,700
78	2.56	256	800
156	1.28	128	400
313	0.64	64	200
625	0.32	32	100
1250	0.16	16	50

It is important to note that if a driver does not offer controlled rise times, then the transmission line effects must be considered even at shorter distances. For example, a driver with a 10ns rise time is affected by distributed transmission line characteristics at a distance as short as one meter, regardless of the bit rate.

Bus Topology

A bus topology is one in which individual transceivers or nodes are connected along a single continuous medium (bus) with a specified upper limit placed on the distance from each node to the bus. A node (N in Figure 4 below) is attached to the bus with a tap or stub. Both ends of the bus must be electrically terminated with the proper passive termination network as described below.

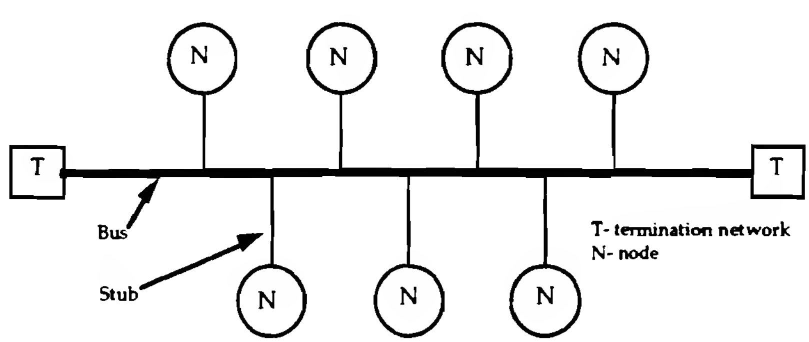


Figure 4. Bus Topology

Characteris Impedance

A cable's characteristic impedance is typically quoted as a single value, i.e., $Z_O = 100\Omega$. In practice, a cable's characteristic impedance is a function of frequency. In general, the characteristic impedance of a cable is given by:

$Z_O = \sqrt{[(r+j2\pi fl)/(g+j2\pi fc)]}$, where,

l = incremental cable inductance

r = incremental cable resistance

g = incremental cable conductance

c = incremental cable capacitance

f = frequency

At high frequencies (over 1 MHz), the characteristic impedance is given by:

$$Z_O = \sqrt{(l/c)}$$

For a given bit and error rate, the length of a network can be maximized by the use of the following guidelines:

- Terminations with impedance equal to the characteristic impedance of the cable, Z_O, should be used at both ends of the bus;
- The receive mode input impedance of the transceivers should be much higher than Z_O in the frequency band of interest;
- The transceivers should be located as close to the bus as possible, with minimal stub lengths.

Departure from these guidelines causes varying degrees of signal reflection and waveform distortion. Excessive waveform distortion can ultimately result in data errors.

Figure 5 is a graph of the actual measured complex impedance of the LONWORKS 22 AWG twisted-pair wire. A manufacturer's specified Z_O is normally the high-frequency asymptote of Z_O. For twisted-pair cables, Z_O is frequently quoted at 1 MHz and is typically around 100Ω, although many specified frequencies are intentionally higher or lower depending on the frequencies being transmitted.

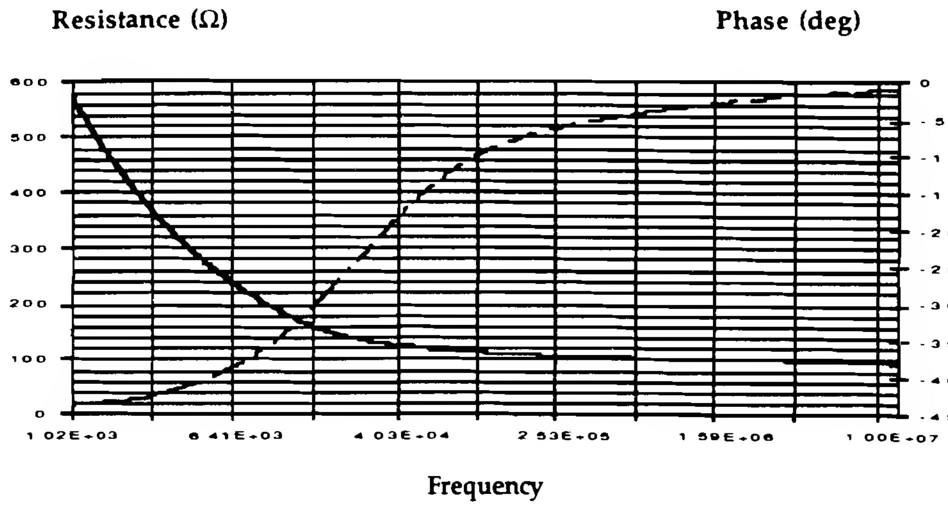


Figure 5. Typical Impedance and Phase Curves of a Twisted Pair Line

Signal-to-Noise Ratio

The signal level at the receiver is determined by both the transmission power and the attenuation of the transmission line. Transmission line attenuation is caused primarily by resistive losses in the copper conductors. Losses due to the dielectric characteristics of the insulation are not generally dominant. These resistive losses, in dB, are proportional to the square root of the frequency due to the skin effect which causes currents to flow more predominantly on the outer surface of the wire at higher frequencies.

Typical attenuation values for 22AWG solid copper twisted pair cable are as follows:

5.5dB / 1,000 ft @ 1MHz
1.5dB / 1,000 ft @ 60KHz

Electrical noise affects the receiver as a function of the coupling strength of unwanted signals with the transmission line, and receiver characteristics such as bandwidth and common-mode rejection. Undesired signal coupling on to a balanced twisted pair cable is primarily common-mode, i.e., coupled equally to both conductors. Thus, a receiver with good common-mode rejection is able to *receive* the intended signal while rejecting the common-mode interference. In actual practice, even if both conductors are subject to the same interference signals, imbalances in the cable result in interference at a receiver that is almost never entirely common-mode.

Typically, a twisted pair cable may be balanced to within 1%, resulting in a differential interference (which the receiver cannot reject) of about 40dB below its common-mode counterpart (which the receiver can reject). Since the resultant noise at the receiver will still be a function of the noise in the operating environment, selection of the best receiver hysteresis threshold is not always obvious: a higher threshold allows for more noise immunity while a lower threshold allows longer bus distances in sufficiently quiet environments.

The performance of the transceivers discussed in this document is predicated on the use of twisted pair cable with tightly controlled specifications. The transceivers described in the document are designed to use Level IV, 22AWG cable. Level IV cable should be used both for the primary data bus as well as for stubs. For recommended wiring connectors, review the document *Connector and Wiring Guidelines For Typical LONWORKS™ Networks* available from Echelon.

Recommended Twisted Pair Transceiver Designs

Overview

Performance specifications for the differential, RS-485, and transformer-coupled transceivers are summarized in Table 6. It should be noted that these specifications are benchmarks, and that actual network performance depends on the tolerance and temperature of the wire used, power supply tolerance, NEURON CHIP tolerance, receiver characteristics, and temperature of the nodes.

Table 6. Performance Summary for Recommended Twisted Pair Transceivers

	Differential	**RS-485**	Transformer -Coupled	
	1.25Mbps	39kbps	78kbps	1.25Mbps
Maximum Typical Distance (m)	30	1200	2000	500
Maximum Typical Stub Length (m)	0.3	0	3	0.3
Maximum Number of Nodes	64	32	64	64
Wire Gauge (AWG)	22	22	22	22
Common-Mode Range 60Hz	0.9V to 3.25V[1]	-7 to +12V	$277V_{RMS}$	$277V_{RMS}$
DC Isolation	None	None	Transformer	Transformer
Power Loss Network Protection	None	High Impendance	Relay	Relay

[1] Unspecified hysteresis

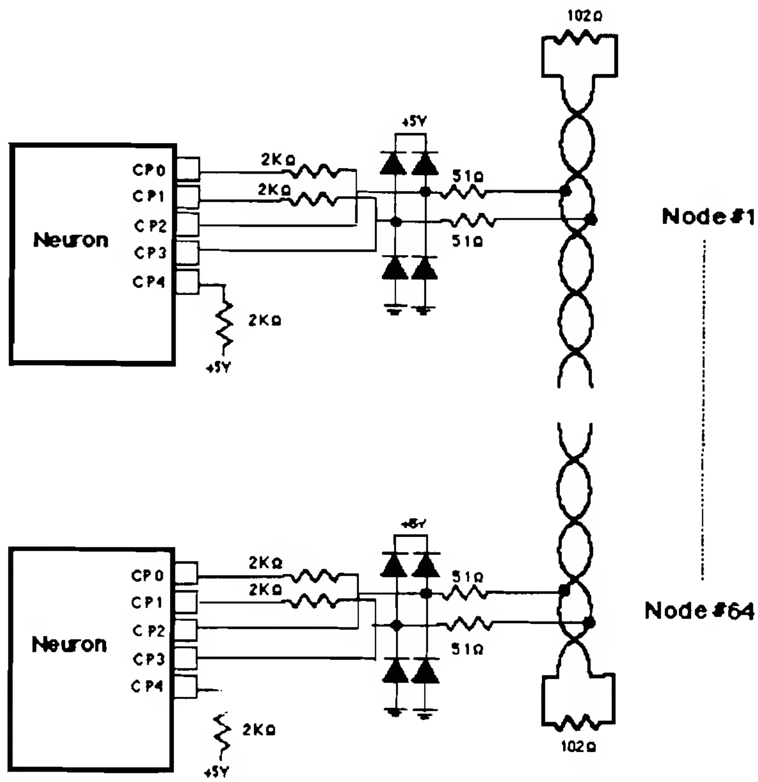
Differential Direct-Connect Twisted Pair Transceiver

The direct-connect transceiver uses the high current output transceiver circuitry integral to the NEURON CHIP to drive the network directly. The differential mode of operation provides some immunity from common-mode noise. This transceiver design is intended for applications in which the LONWORKS nodes are in close proximity, typically less than 30 meters.

Figure 6 presents the schematic of a direct-connect twisted pair transceiver. The communications port of the NEURON CHIP provides direct connection to a small twisted pair network. Each end of the twisted pair cable must be terminated with a 102 Ω resistor to match the characteristic impedance of the line. Failure to do so causes reflections which interact with the main signal, resulting in cancellations or false signals that can lead to reception failure at higher data rates. The four 1N4148 diodes are connected to protect the NEURON CHIP from small transients that could be picked up from the twisted pair cable.

This direct-connect network has a common-mode voltage range from 1.2V to V_{DD} - 2.2V with specified hysteresis. The expected transmission range may be up to 30 meters for any of the available transmission rates from 1.25Mbps. In most cases, the transmission distance will be limited by common-mode range effects. It is important when using this circuit to insure that all of the nodes have a common ground. The amplitude of the transmitted signal will be about 3.3 V peak-to-peak.

If the nodes are interconnected using printed circuit board wiring, it is best to keep the characteristic impedance of the traces at 102Ω.



Resistors: 1%,100PPM per ° C, metal film, 1/8 Watt

Figure 6. Differential Direct-Connect Twisted Pair Transceiver Schematic

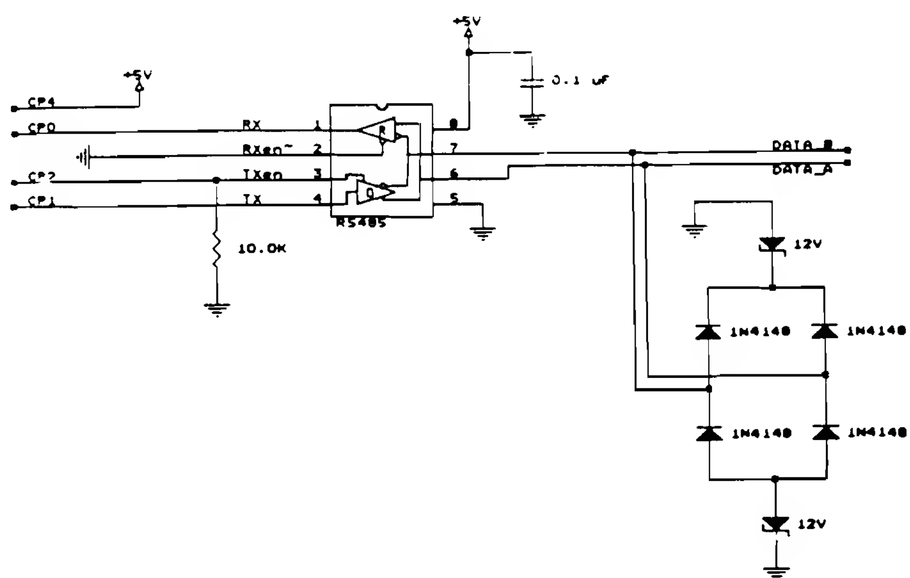
RS-485 Transceiver

The RS-485 transceiver supports the EIA RS-485 electrical specifications for signalling. The RS-485 standard allows for a continuum of bit rates. The transceiver presented below must be set to 39kbps operation to meet the specifications listed in Table 6. The RS-485 standard specifies that the node be connected directly to the twisted pair cable without a wire stub, and this can be effected by using a daisy chain wiring technique.

Three optical isolators can be used when isolation is required between the twisted pair cable and the transceiver: one for the transmit signal, one for the receive signal, and a third for the transmit enable signal. The designer should be certain that the response time is sufficiently fast to support the selected bit rate. The RS-485 transceiver local ground must be referenced to the local ground of the other RS-485 transceivers operating on the same network. Consult the EIA RS-485 specification A.3 for additional information.

Figure 7 presents the schematic for an RS-485 transceiver. This schematic is for the transceiver used in Echelon's TP-RS485 Twisted Pair Control Module.

The RS-485 transceiver must be terminated at both ends with either the complex termination shown in Figure 8, or with a 121Ω, 1%, 100PPM per °C, metal film, 1/8 watt resistor in order to minimize reflections.



NOTES

1. RS-485 transceiver chip is TI SN75LBC176.

2.Unless otherwise noted, the following ratings apply:

Capacitor: -20,+80%, Z5U, 50V, ceramic

Resistor: 5%, metal film, 1/8 Watt

Figure 7. RS-485 Twisted Pair Transceiver Schematic

Transformer-Coupled Transceivers

Transformer isolation increases immunity to common-mode noise and also addresses ground loop problems found in distributed systems such as networks. Different transformers are used for the two transceivers presented below: 78kbps and 1.25Mbps. These transformers have been designed to provide the optimal isolation, drive, and impedance for each bit rate. These transformers are available from the following sources:

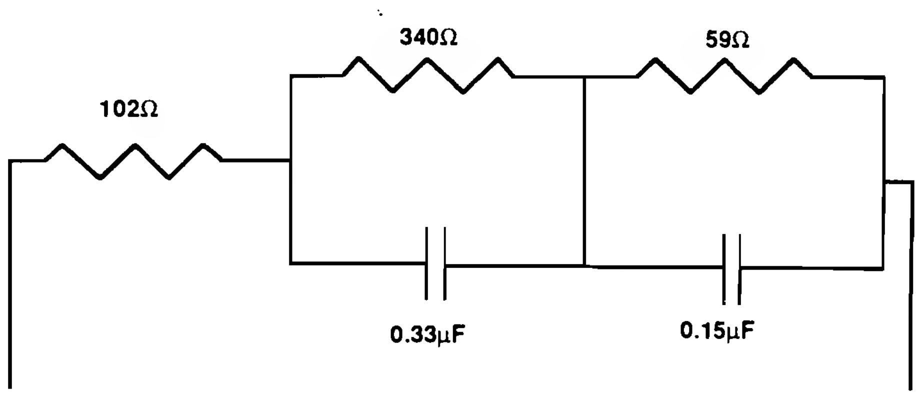
78kbps: Precision Components, Inc.
710 Western, Suite B
Lombard, IL. 60148
1-708-543-6448
Part No. PCI 0505-0542

1.25Mbps: Pulse Engineering, Inc.
P.O. Box 12235
San Diego, CA. 92112
1-619-674-8100
Part No. PE-65948

In order to meet minimum input impedance requirements for 78kbps and 1.25Mbps transformer-coupled nodes, the differential capacitance from the twisted pair medium tap connector to the transceiver must be kept within a maximum limit specified in the table below:

Transceiver Type	Maximum mutual data pair conductor capacitance from medium tap connector to node transceiver
78kbps	5 pF
1.25Mbps	2 pF

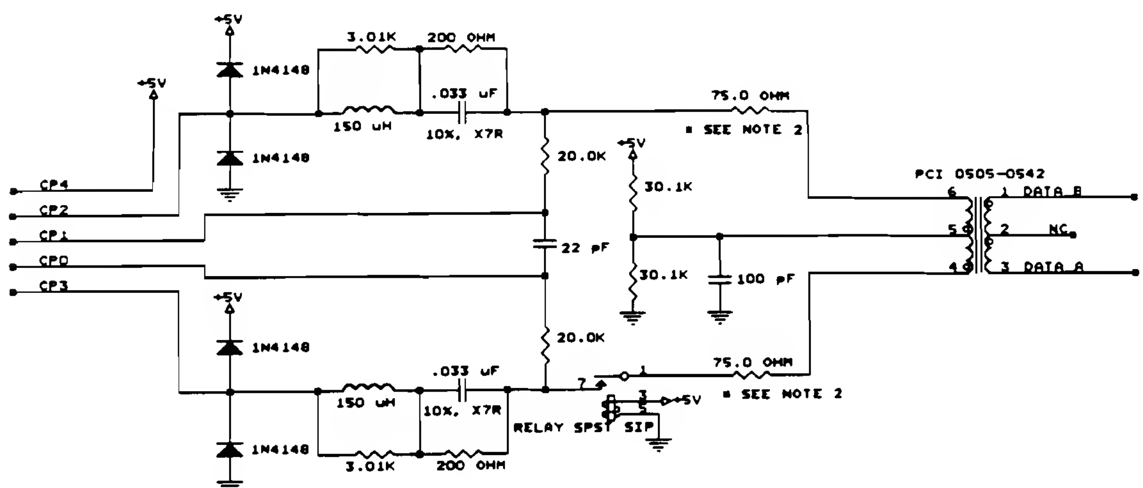
The termination circuit shown in Figure 8 below is optimized to match the characteristic impedance of the twisted pair transceivers for bit rates of 39kbps to 1.25Mbps. The twisted pair data bus must be terminated at each end to minimize reflections.



Capacitors: 10%, 50V, metal polyester Resistors: 1%,100PPM per ° C, metal film, 1/8 Watt

Figure 8. Termination Circuit for RS-485, 78kbps, and 1.25Mbps Transceivers

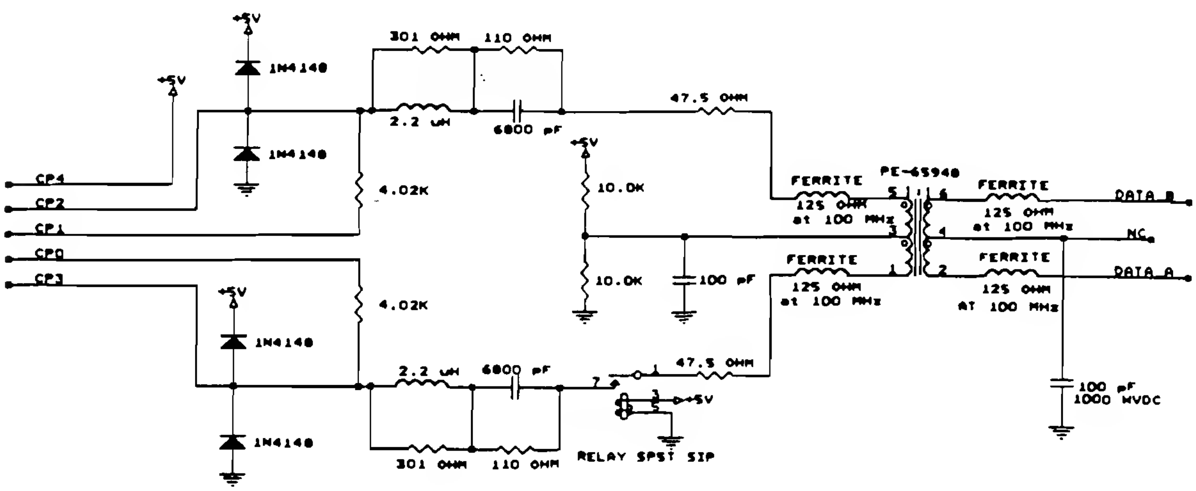
Figures 9 and 10 present the schematics for 78kbps and 1.25Mbps transformer-isolated transceivers, respectively. These schematics are similar to the transceivers used in Echelon's TP/XF-78 and TP/XF-1250 Twisted Pair Control Modules, respectively.



NOTES

1. Unless otherwise noted, the following ratings apply:
   Capacitors: 5%, NPO, 50V, ceramic
   Resistors: 1%,100PPM per ° C, metal film, 1/8 Watt
   Inductors: 5%
2. The value of this resistor should be such that the combined typical DC resistance of this resistor and the 150μH inductor equals 78Ω.

Figure 9. Transformer-Isolated 78kbps Twisted Pair Transceiver



NOTES

1. Unless otherwise noted, the following ratings apply:

Capacitors: 5%, NPO, 50V, ceramic

Resistors: 1%,100PPM per ° C, metal film, 1/8 Watt

Inductors: 5%

Figure 10. Transformer-Isolated 1.25Mbps Twisted Pair Transceiver

Summary

This document describes four methods of implementing twisted pair transceivers for LONWORKS networks. One method uses the differential driver circuitry of the NEURON CHIP, and is most appropriate for short distance communications, i.e., between nodes operating over a circuit board backplane or within a machine or other device. The RS-485 transceiver is best used for short to medium distance industrial applications with limited common-mode noise. The two transformer-isolated designs operate well in the presence of common-mode noise, and are therefore well suited for industrial and building control applications.

This document is not intended to be an exhaustive guide to twisted pair transceivers. The designs presented in this guide have been well researched and tested by Echelon, and are proven in terms of their performance. As new designs are reviewed by Echelon, this guide will be expanded accordingly.

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